



10/023,819

PATENT

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Biju Chandran et al. Examiner: John Vigushin  
Serial No.: 10/023,819 Group Art Unit: 2827  
Filed: December 21, 2001 Docket: 884.A27US1  
Title: CHIP JOIN PROCESS TO REDUCE ELONGATION MISMATCH BETWEEN  
THE ADHERENTS AND SEMICONDUCTOR PACKAGE MADE THEREBY

Assignee: Intel Corporation Customer No: 21186

**AMENDMENT UNDER 37 C.F.R. § 1.312(a)**

Mail Stop Issue Fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

In response to the Notice of Allowance mailed April 25, 2005, please amend the above-identified application as follows:

OK to ENTER - Ex. John B. Vigushin  
06/13/06